Product Definition

Ultra-low power Wearable, Optical ,Heart-Rate Sensor，SpO2 and Proximity Sensor with I 2C Interface .

Description

HX4101 is an ultra-low power wearable, optical, heart-rate monitor and Proximity sensor with I2C Interface. HX4101 include Transmitter and Receiver two parts . The Transmitter supports two green switching light-emitting diode (LED) 、one Red LED and one Infrared LED ; The Receiver have a photodiode、AFE and a high resolution ADC . Heart rate Sensor is designed to monitor heart rate by PPG reflective method with DC cancellation scheme . The proximity sensing is realized by Infrared LED, a proximity detection photodiode, programmable pulse LED driver circuit . The current from the photodiode is digitized using an analog-to-digital converter (ADC). The ADC code can be read out using an I2C interface. HX4101 have three fully-integrated LED driver with a 8-bit current control. The device has a high dynamic range transmit and receive circuitry that helps with the sensing of very small signal levels .

Features

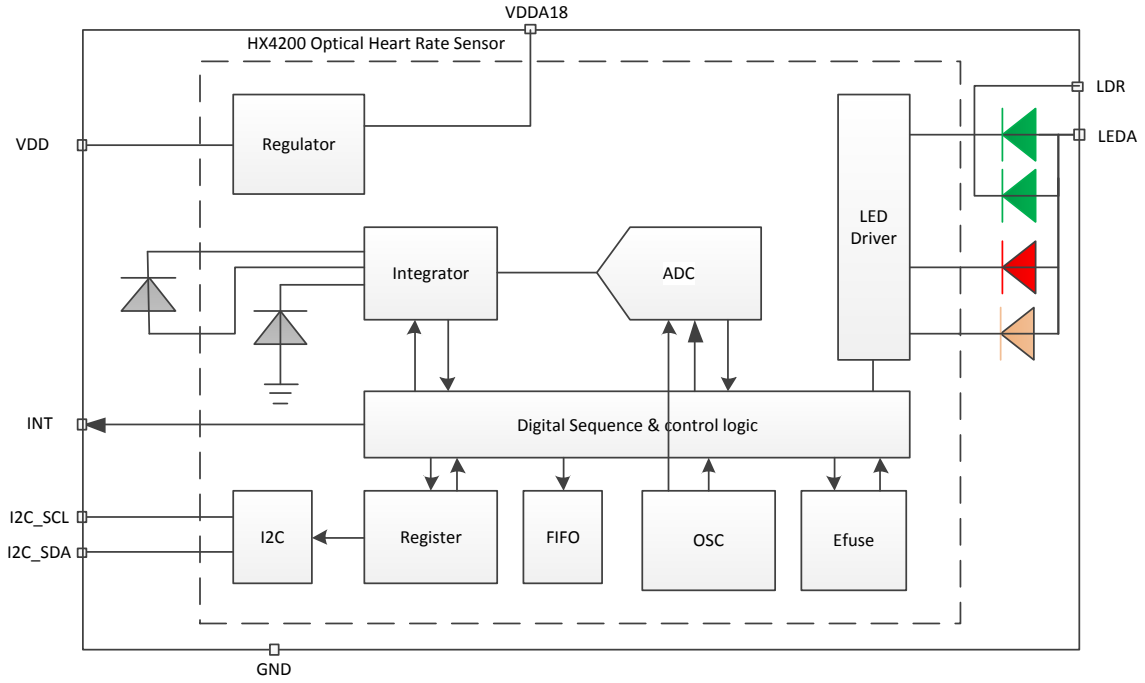
- **Transmitter:**
  - Dynamic Range: 102 dB
  - 8-Bit Programmable LED Current from 0.78mA to 50 mA (Extendable to 200 mA)
  - Support LED Pulse driving: Programmable Both Duty cycle and Width
  - Support of two green LED for optimized HRM
  - Support of Red LED and IR LED for SpO2
  - Support of IR LED for Proximity sensor
- **Receiver:**
  - 24-Bit Representation of the Current Input from a Photodiode in Twos Complement Format
  - Photodiode size 1.27*1.27mm
  - Programmable Gain from 1 to 128 (Cgain_max=128*Cgain_min)
  - Dynamic Range: 98dB

- **Pulse Sample Frequency: 10 SPS to 1000 SPS**
- **HX4101 Ultra-low power Heart Rate Static monitor 200uA**
- **Interface: I2C BUS up to 800KHz**
- **Operating Temperature Range: -20℃ to 85℃**
- **Supplies: Rx: 2 V to 3.6 V, Tx: 3 V to 5.25 V**
- **Package size :7.7mm×4.8mm×1.1mm**

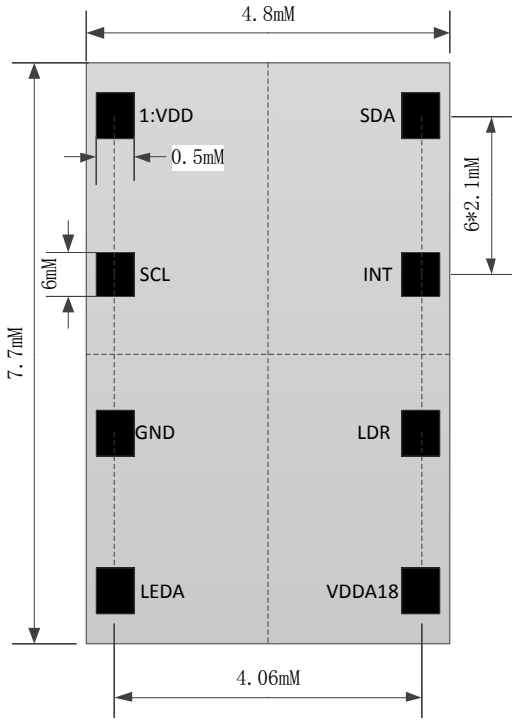
Applications

- Optical Heart-Rate Monitoring (HRM)
- Optical Heart-Rate Variability (HRV)
- Proximity Detect (PS)
- SpO2
- Blood Pressure (BP)

Function Block Diagrams



Pin Configuration



TOP VIEW

PIN LIST :

Pin	Name	Type	Description
1	VDD	A	Power supply; 1-μF decapacitor to GND
2	SCL	D	I2C CLK, external pull up resistor (for example, 10 k Ω)
3	GND	A	Common ground for transmitter and receiver
4	LEDA	A	Anode of led , connect toVDD
5	VDDA18	A	Internal 1.8V LDO output pin ,only need 1-μF capacitor to GND
6	LDR	A	LED driver pin ;floating in normal work
7	INT	D	ADC ready interrupt signal (output)for HRM and INT signal for PS
8	SDA	D	I2C data, external pull up resistor (for example, 10 k Ω)

Specifications

Absolute Maximum Ratings(T_a=25℃,unless otherwise specified)

Parameter	Min	Max	Unit
VDD	-0.2	4	V
LEDA	-0.2	6	
Analog inputs	VDD – 0.3	VDD + 0.3	V
Digital inputs	VDD – 0.3	VDD+ 0.3	V
Input current to any pin except supply pins		±7	mA
Operating temperature range	-20	85	℃
Maximum junction temperature		125	

Recommended Operating Conditions

	Min	Max	Unit
VDD	2	3.6	V
LEDA	3	5.5	V
Supply voltage accuracy	±5		%
Specified temperature range	-20	85	℃
Maximum junction temperature		125	

ESD Ratings

		Value	Unit
V(esd) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101	±250	

Electrical Characteristics

Minimum and maximum specifications are at T_A = –20°C to 85°C, typical specifications are at 25°C.VDD=3.3V, 25 Hz date output rate , LED driver current 25mA, pulse frequency = 31.25KHz , 25% Duty cycle , 4MHz internal clock ,unless otherwise noted .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PULSE REPETITION FREQUENCY					
PRF(1) Pulse repetition frequency		**10**		**1000**	**SPS**
RECEIVER					
Offset cancellation DAC current range	8bits IDAC		**-7.5 to 7.5**		**uA**
Offset cancellation DAC current step			**30**		**nA**
First integrator gain setting (Cint)	Cint=78fF to 20pF		**1 to 256**		
TRANSMITTER					
LED current range	**ILED_RG<1:0>=1**		**0 to 50**		**mA**
	ILED_RG<1:0>=2		**0 to 100**		
	ILED_RG<1:0>=3		**0 to 200**		
LED current resolution			**8**		**Bits**
CLK (Internal Oscillator)					
Frequency			**4**		**MHz**
Accuracy	Room temperature		**±1%**		
Frequency drift with temperature	Full temperature range		**±0. 5%**		
Jitter (RMS)			**100**		**pS**
I2C INTERFACE					
Maximum clock speed			**800**		**KHz**
I2C slave address			**0x44**		**HEX**
PERFORMANCE					
Receiver SNR			**102**		**dB**

Transmitter SNR		**98**	**dB**
CURRENT CONSUMPTION			
RX VDD current	Normal operation	**100**	**uA**
	Hardware power-down mode	**3**	**uA**
TX LED current	Normal operation	**80**(2)	**uA**
	Hardware power-down mode	**3**	**uA**
I2C BUS current	R_PULL = 10k	**80**	**uA**
DIGITAL INPUTS			
V_{IH} High-level input voltage		**0.9*VDD VDD**	**V**
V_{IL} Low-level input voltage		**0 0.1*VDD**	**V**
DIGITAL OUTPUTS			
V_{OH} High-level output voltage		**VDD**	**V**
V_{OL} Low-level output voltage		**0**	**V**

(1) PRF refers to the rate at which samples from each of the two phases are output from the AFE.

(2) I_tx = 25mA*1.25%*25%=80uA , 1.25%= Ts_adc/PRF，25%= Ts_led_on/Ts_led_pulse

Low Power consumption

24bits adc Ts_adc=500uS , duty1=Ts_adc/PRF , duty2=Ts_led_on/Ts_led_pulse , Idd(VDD) =300uA* duty1 , Idd(TX_SUP) =25mA* duty1*duty2

PRF (SPS) Hz	Idd(VDD) uA	Idd(TX_SUP) uA	Description
25	100	80	LED Pulse Frequency = 31.25KHz, duty cycle = 25%
50	115	160	LED Pulse Frequency = 31.25KHz, duty cycle = 25%
100	145	320	LED Pulse Frequency = 31.25KHz, duty cycle = 25%
200	165	640	LED Pulse Frequency = 31.25KHz, duty cycle = 25%
1000	250	1280	LED Pulse Frequency = 31.25KHz, duty cycle = 12.5%
1000	250	3125	LED Pulse Frequency = 31.25KHz, duty cycle = 25%

Green LED Characteristics

Parameter	Min	Typ.	Max	Units	Description
V_F		2.7	3.0	V	LED Forward Voltage, I_F=20mA
V_R	5			V	LED Reverse Voltage, I_R=10μA
P_O	3.0			mW	LED Radiant Power, I_F=20mA
λ_p		520		nm	LED peak wavelength, I_F=20mA
Δ_λ		50		nm	Spectral Radiation Bandwidth
T_R		25		ns	LED optical Rise time, I_F=20mA
T_F		13		ns	LED optical Fall time, I_F=20mA

Feature Description

Input integrator and DC cancellation IDAC

The input pins of integrator are meant to be connected differentially to a internal or external photodiode , The signal current from the photodiode is integrated in every ADC conversion time . There are also a DC cancellation scheme which is realized SAR logic and 8 bits IDAC. the whole system operating in cancellation scheme when cancellation signal is high . the cancellation signal is controlled by both 1bits register .

LED Current Setting

The default LED current range is from 0 mA to 50 mA. Taken as a decimal number, the 8-bit setting provides 256 equal steps between 0 mA and 50 mA. Each increment of the ILED 8-bit code causes the LED current setting to increment by approximately 0.2 mA.

The LED current range can be doubled by setting the ILED_2X bit to 1. The accuracy of higher current settings close to 200 mA can be low because of current saturation of the driver. Each increment of the ILED 8-bit code causes the LED current to increment by approximately 0.8 mA when ILED_2X is set to 1.

Analog-to-Digital Converter (ADC)

The AFE has an ADC that provides a 24-bit representation of the current from the photodiode. The ADC codes corresponding to the sampling phase can be read out from 24-bit registers in twos complement format.

I²C Protocol

Interface and control are accomplished through an I²C serial compatible interface to a set of registers that provide access to device control functions and output data. The address of HX4101 is 0x44, the device also supports the 7-bit I²C addressing protocol. HX4101 supports the standard writing and reading protocol. The register index will automatically increase by 1 after the addressed register has been accessed (read or write).

A Acknowledge (0)

P Stop Condition

R Read (1)

S Start Condition

W Write (0)

Sr Repeated Start Condition

■ Master-to- Slave

□ Slave-to-Master

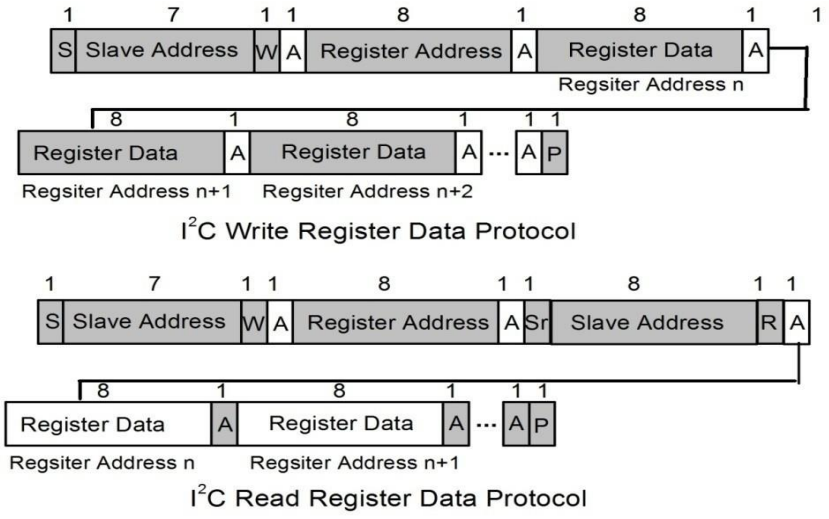


Figure 2. I²C Protocols

Register List

The device is controlled and monitored by data registers accessible through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Table 1.

Table 1. Register Address

Address	name	R/W	function	Recommend Value
0x00	ID	RO	Device ID	0x41
0x01	Rev_ID	RO	RA_REV_ID	0x01
0x02	Sleep enb	R/W	Sleep function enable	0x30
0x03	HRS DATA1	RO	hrs_data1_out [7:0]	0x00
0x04		RO	hrs_data1_out [15:8]	0x00
0x05		RO	hrs_data1_out [23:16]	0x00
0x06	HRS DATA2	RO	hrs_data2_out [7:0]	0x00
0x07		RO	hrs_data2_out [15:8]	0x00
0x08		RO	hrs_data2_out [23:16]	0x00
0x09	HRS DATA1 - HRS DATA2	RO	hrs_data1_2_out [7:0]	0x00
0x0A		RO	hrs_data1_2_out [15:8]	0x00
0x0B		RO	hrs_data1_2_out [23:16]	0x00
0x0C	PS1 DATA1	RO	ps1_data1_out [7:0]	0x00
0x0D		RO	ps1_data1_out [15:8]	0x00
0x0E		RO	ps1_data1_out [23:16]	0x00
0x0F	PS1 DATA2	RO	ps1_data2_out [7:0]	0x00
0x10		RO	ps1_data2_out [15:8]	0x00
0x11		RO	ps1_data2_out [23:16]	0x00
0x12	PS1 DATA1 - PS1 DATA2	RO	ps1_data1_2_out [7:0]	0x00
0x13		RO	ps1_data1_2_out [15:8]	0x00
0x14		RO	ps1_data1_2_out [23:16]	0x00
0x15	PS2 DATA1	RO	ps2_data1_out [7:0]	0x00
0x16		RO	ps2_data1_out [15:8]	0x00
0x17		RO	ps2_data1_out [23:16]	0x00
0x18	PS2 DATA2	RO	ps2_data2_out [7:0]	0x00
0x19		RO	ps2_data2_out [15:8]	0x00
0x1A		RO	ps2_data2_out [23:16]	0x00
0x1B	PS2 DATA1 -	RO	ps2_data1_2_out [7:0]	0x00

0x1C	PS2 DATA2	RO	ps2_data1_2_out [15:8]	0x00
0x1D		RO	ps2_data1_2_out [23:16]	0x00
0x1E	PS3 DATA1	RO	ps3_data1_out [7:0]	0x00
0x1F		RO	ps3_data1_out [15:8]	0x00
0x20		RO	ps3_data1_out [23:16]	0x00
0x21	PS3 DATA2	RO	ps3_data2_out [7:0]	0x00
0x22		RO	ps3_data2_out [15:8]	0x00
0x23		RO	ps3_data2_out [23:16]	0x00
0x24	PS3 DATA1 - PS3 DATA2	RO	ps3_data1_2_out [7:0]	0x00
0x25		RO	ps3_data1_2_out [15:8]	0x00
0x26		RO	ps3_data1_2_out [23:16]	0x00
0x2A	FIFO	R/W	fifo_watermark_i2c[5:0]	0x18
0x2B	FIFO	R/W		0x22
0x2D	FIFO_DATA	R0	FIFO _dataout[7:0]	0X00
0x2E	FIFO_DATA	R0	FIFO _dataout[15:8]	0X00
0x2F	FIFO_DATA	R0	FIFO _dataout[23:16]	0X00
0x30	Enable	R/W	HRS/PS1 ENABLE	0X33
0X31	Enable	R/W	PS1/PS2 ENABLE	0X33
0x32	PRF	R/W	prf_cycle_i2c[7:0]	0x00
0x33	PRF	R/W	prf_cycle_i2c[15:8]	0x71
0x34	PRF	R/W	prf_cycle_i2c[23:16]	0x02
0xB8	LED	R/W	LED range set	Ox56
0xB9	LED1	R/W	Led1 drive current set	0x00
0xBA	LED2	R/W	Led2 drive current set	0x00
0xBB	LED3	R/W	Led3 drive current set	0x00

ID Register(0x00)

The ID Register(read-only) provides the value for the part number.

BITS	FIELD	Description
7:0	ID	0x41

SLEEP Register(0x02)

The Sleep register is used to enable and disable the chip ,when sleep function is enabled , I_vdd<1uA.

BITS	FIELD	Description

7:2	Reserved	Reserved
0	Sleep	1:power down; 0:power on

FIFO related Register (0x2A)

Fifo_watermark_i2c, which is used for setting the number of almost full interrupt ;

BITS	**FIELD**	**Description**
7:6	Reserved	Reserved
5:0	fifo_watermark_i2c[5:0]	fifo_watermark_i2c[5:0]

FIFO related Register (0x2B)

fifo_data_sel_i2c/ fifo_int_clr_mode_i2c/ fifo_mode_i2c ;

BITS	**FIELD**	**Description**
7:4	fifo_data_sel_i2c	0x0: hrs_data1 0x1: hrs_data2 0x2: hrs_data1 - hrs_data2 0x3: ps1_data1 0x4: ps1_data2 0x5: ps1_data1 - ps1_data2 0x6: ps2_data1 0x7: ps2_data2 0x8: ps2_data1 - ps2_data2 0x9: ps3_data1 0xA: ps3_data2 0xB: ps3_data1 - ps3_data2
3:2	fifo_int_clr_mode_i2c	0x0：self clear 0x1：reserve 0x2：manual clear 0x3：reserve
1:0	fifo_mode_i2c	0x0：bypass 0x1：FIFO 0x2：stream

		0x3：reserve

FIFO related Register (0x2D/0X2E/0X2F)

BITS	FIELD	Description
0x2D <7:0>	Fifo_data<7:0>	Read only
0x2E<7:0>	Fifo_data<15:8>	Read only
0x2F <7:0>	Fifo_data<24:16>	Every time write this register ,FIFO pull out a new data

HRS Enable / PS1 Enable Register (0X30)

BITS	FIELD	Description
7	PS1_enable	1 PS1 enable ; 0 PS1 disable
6:4	PS1 ADC ORS Set	0x0 ： 128 0x1 ： 256 0x2 ： 512 0x3 ： 1024 0x4 ： 2048 other： reserve
3	HRS_enable	1 HRS enable ; 0 HRS disable
2:0	HRS ADC ORS Set	0x0 ： 128 0x1 ： 256 0x2 ： 512 0x3 ： 1024 0x4 ： 2048 other： reserve

PS2 Enable / PS3 Enable Register (0X31)

BITS	FIELD	Description
7	PS3_enable	1 PS3 enable ; 0 PS3 disable
6:4	PS3 ADC ORS Set	0x0 ： 128

		0x1 ： 256 0x2 ： 512 0x3 ： 1024 0x4 ： 2048 other： reserve
3	PS2_enable	1 PS2 enable ; 0 PS2 disable
2:0	PS2 ADC ORS Set	0x0 ： 128 0x1 ： 256 0x2 ： 512 0x3 ： 1024 0x4 ： 2048 other： reserve

LED DRIVER RANGE SET REGISTER (0Xb8)

BITS	FIELD	Description
7:6	LED3DR_RG<1:0>	01 LED 0~50mA 10 LED 0~100mA 11 LED 0~200mA
5:4	LED2DR_RG<1:0>	01 LED 0~50mA 10 LED 0~100mA 11 LED 0~200mA
3:2	LED1DR_RG<1:0>	01 LED 0~50mA 10 LED 0~100mA 11 LED 0~200mA
1:0	Reserved	Reserved

Application Information

A typical application for HX4101 is shown in Figure 8. The I^2C signals and the Interrupt are open-drain outputs and require pull-up resistor (R_P). It is recommended use 10 kΩ resistor when running at 400kbps. A 10 KΩ pull up resistor (R_{PI}) can be used for the interrupt line.

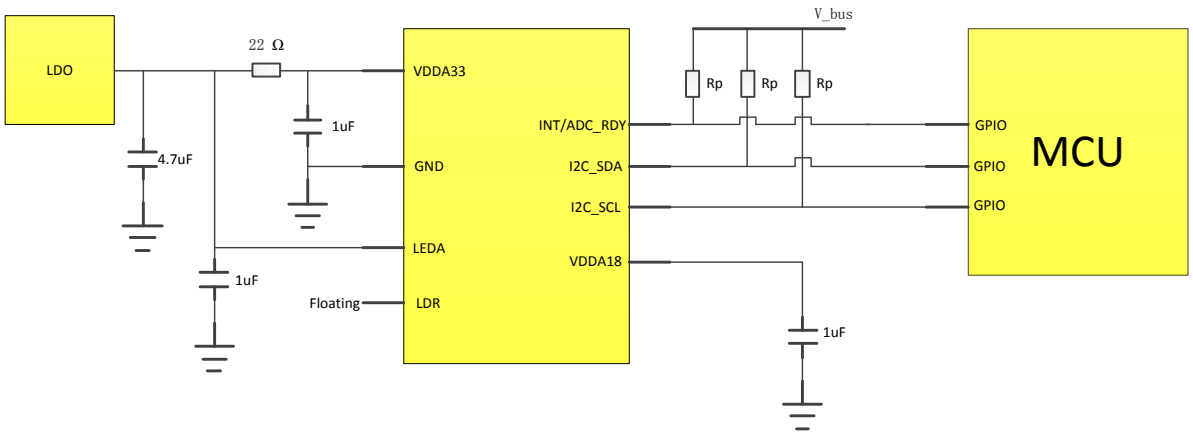


Figure 8. Typical Application Schematic Diagram

PCB Pad Layout

Suggest PCB pad layout guidelines for the surface module are shown in Figure 9.

Flash Gold is recommended surface finish for the landing pads.

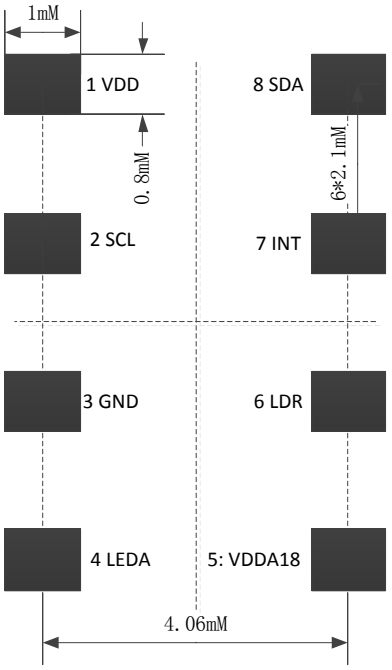
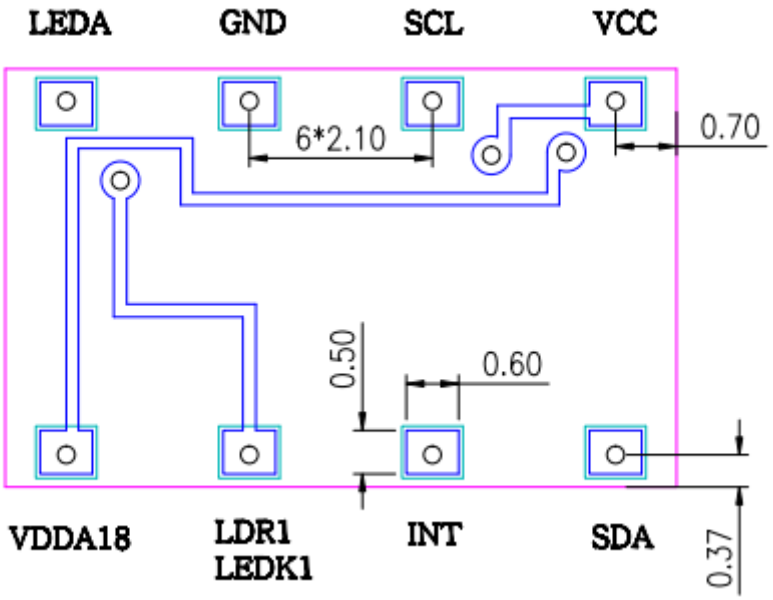


Figure 9. Suggested Module PCB layout
Note: All linear dimensions are in mm

Package Information
size : 7.7*4.8*1.1mM



Bottom view